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PATENT APPLICATION
Q59017

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

4/12/01

U. Hart

In re application of

Shigeru SEMBONMATSU, et al.

Appln. No.: 09/559,348

Group Art Unit: 3728

Confirmation No.: Not yet known.

Examiner: Shian T. Luong

Filed: April 27, 2000

For: TRAY FOR SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

AMENDMENT UNDER 37 C.F.R. §1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated January 23, 2001, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claim 2 without prejudice and/or disclaimer.

Please enter the following amended claim:

1. (Amended) A tray for storing a semiconductor integrated circuit device having a package and wiring terminals on a lower surface of the package, said tray comprising:

a substantially planar main body; and

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a first storage portion provided on a first surface of said main body for storing the semiconductor integrated circuit device, said first storage portion having a first wall surface adapted to be arranged around the semiconductor integrated circuit device when the semiconductor integrated device is stored in said first storage portion,

wherein said first wall surface has a first area and a second area, said first area being inclined at an angle so as to support an edge of the package of the semiconductor integrated circuit device and to prevent said first wall surface from coming into contact with the wiring terminals of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said first storage portion, and said second area extending from said first area in a direction away from said first surface of said main body, wherein said second area is inclined at an angle larger than the angle of first area.

Please add the following new claims:

9. 10. (New) A tray according to claim 1, wherein said first area is inclined at an angle between 40 degrees and 70 degrees.

10. 11. (New) A tray according to claim 1, wherein said second area is inclined at an angle between 85 degrees and 90 degrees.

24

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11/12. (New) A tray according to claim 1, wherein said first area is inclined at an angle between 40 degrees and 70 degrees, and said second area is inclined at an angle between 85 degrees and 90 degrees.

Sub 2 13. (New) A tray for storing a semiconductor integrated circuit device having a package and wiring terminals on a lower surface of the package, said tray comprising:

a substantially planar main body;

a first storage portion provided on a first surface of said main body for storing the semiconductor integrated circuit device, said first storage portion having a first wall surface adapted to be arranged around the semiconductor integrated circuit device when the semiconductor integrated device is stored in said first storage portion, wherein said first wall surface has a first area which is inclined at an angle so as to support an edge of the package of the semiconductor integrated circuit device and to prevent said first wall surface from coming into contact with the wiring terminals of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said first storage portion; and

a second storage portion provided on a second surface of said main body opposite to said first storage portion, wherein said second storage portion can store a semiconductor integrated circuit device with wiring terminals thereof facing upward when said tray is turned over, and

wherein when two of said trays are aligned in a stacked relationship, said second storage portion of one tray cooperates with said first storage portion of the other tray to form a space for storing the semiconductor integrated circuit device.

13
14. (New) A tray according to claim 13, wherein said second storage portion has a second wall surface adapted to be arranged around the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said second storage portion with the wiring terminals thereof facing upward, and

wherein said second wall surface has a third area which is inclined at an angle so as to support an edge of the package of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said second stage portion.

14
15. (New) A tray according to claim 13, further comprising positioning means for positioning said stacked trays to each other.

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16. (New) A tray according to claim 13, wherein said main body includes a plurality of projecting pieces provided on said second surface thereof for defining said second storage portion, and wherein each of said projecting pieces has a wall surface for serving as said second

AMENDMENT UNDER 37 C.F.R. §1.111
U.S. Appln. No. 09/559,348

Our Ref.: Q59017
Art Unit: 3728

the rectangular package of the semiconductor integrated circuit device.

Figure 1. Schematic representation of the experimental design. The figure shows a vertical timeline of the study. At the top, 'Baseline' is indicated. Below this, 'Pre-Test' is shown. The main part of the study is divided into two groups: 'Control' and 'Intervention'. The 'Control' group receives 'Control' and 'Intervention' treatments. The 'Intervention' group receives 'Intervention' and 'Control' treatments. The timeline ends with 'Post-Test'.

REMARKS

Applicants thank the Examiner for acknowledging Applicants' claim to foreign priority under 35 U.S.C. §119(a)-(d), and for confirming that the certified copy of the priority document has been received at the U.S. Patent and Trademark Office.

Information Disclosure Statement:

In Paper No. 4, Office Action Summary (PTO-326), the Examiner indicates that the Information Disclosure Statement (PTO-1449) provided by Applicants was attached to Paper No. 4, dated January 23, 2001. However, Applicants have not received the above-mentioned copy with the Examiner's initials, thus not confirming that these references have been considered.

Applicants hereby request the Examiner to provide Applicants with a copy of the Form PTO-1449 filed on April 27, 2000, with the Examiner's initials by the cited references prior to or concurrently with the next Official Action in the above-referenced case.

Claim Rejections:

Claims 1-16 are all of the claims pending in the application. Claims 1-9 are the only claims that have been examined, as claims 10-16 are newly added. Presently claims 1-9 stand rejected.

35 U.S.C. §112, 2nd Paragraph Rejection - Claim 2:

As claim 2 has been cancelled, this rejection is now moot.

35 U.S.C. §102(e) Rejection - Claims 1-6 and 8:

Claims 1-6 and 8 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,957,293 to Pakeriasamy. In view of the following discussion, Applicants respectfully traverse the above rejection.

Pakeriasamy discloses a semiconductor tray 11a or 11b that has a plurality of semiconductor chip pockets 24 to carry semiconductor type chips 12. Each of the pockets 24 are defined by a bottom wall 30 and a plurality of side walls 32a through 32d. See Pakeriasamy, col. 4, lines 19-21. "The side walls and end walls 32a-32d are joined integrally to the edges of the bottom wall 30 and extend vertically therefrom so as to form a central cavity portion 36." *Id.* at lines 21-23 (emphasis added). Only in Figure 7 does Pakeriasamy disclose having side walls which are angled to support a substrate. However, at no point does Pakeriasamy discuss this angle or provide any information regarding these side walls except that they extend "vertically" from the bottom wall of the pocket.

Moreover, at no point does Pakeriasamy disclose a wall surface of the pocket that has first and second areas, where the angle of the second area is larger than the angle of the first area, as claimed in claim 1. Figure 7 of Pakeriasamy clearly shows that the walls of the pocket only have a single angled area. At no point does Pakeriasamy disclose having the walls 32a-32d broken into two distinct areas, where one area has a different angle than the other. More particularly, Pakeriasamy does not disclose having the two above-mentioned areas, where the second area has a greater angle than the first area.

Therefore, Applicants respectfully submit that Pakeriasamy fails to teach each and every element of claim 1, and hereby requests the Examiner to reconsider and withdraw the 35 U.S.C. §102(e) rejection of claim 1. Additionally, as claims 3 through 12 depend from claim 1, these claims are also allowable, at least by reason of their dependency.

As new claim 13 is identical to the original claim 6, Applicants will now address the rejection of claim 6 set forth in the Office Action dated January 23, 2001, but with regard to the language of claim 13. Claim 13 recites, *inter alia*, a tray which has a plurality of first and second storage portions, where the second storage portions are provided on the tray opposite the first storage portions. This feature of the present invention is not disclosed in Pakeriasamy. Pakeriasamy merely discloses having a plurality of stand-offs 42 provided out of the bottom of the trays so as to provide a downward force on substrates sitting in the pockets 24 of the other tray. At no point does Pakeriasamy disclose having a plurality of first and second storage portions on a single tray, wherein "the second storage portion can store a semiconductor integrated circuit device with wiring terminals thereof facing upward when [the] tray is turned over." See claim 13.

Therefore, Applicants respectfully submit that Pakeriasamy fails to disclose each and every feature of claim 13, and hereby submits that this claim is in condition for allowance. Moreover, as claims 14-16 depend on claim 13, these claims are also allowable, at least by reason of their dependency.

35 U.S.C. §103(a) Rejection – Claims 7 and 9:

Claims 7 and 9 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pakeriasamy in view of U.S. Patent No. 5,418,692 to Nemoto. Both of these claims depend on claim 6, which depends on claim 1. Since claim 1 has been rejected under 35 U.S.C. §102(e) in view of Pakeriasamy, and Nemoto does not cure the deficient teachings of Pakeriasamy with respect to claim 1, Applicants submit that claims 7 and 9 are allowable at least by reason of their dependency.

Conclusion:

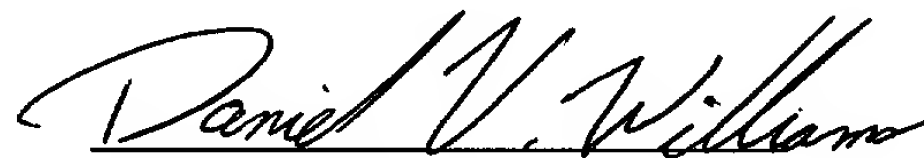
In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the local telephone number listed below.

AMENDMENT UNDER 37 C.F.R. §1.111
U.S. Appln. No. 09/559,348

Our Ref.: Q59017
Art Unit: 3728

Applicants hereby petition for any extension of time that may be required to maintain the pendency of this case, and any required fee (except for the Issue Fee) is to be charged to our Deposit Account No. 19-4880.

Respectfully submitted,



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Date Filed: April 10, 2001



APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 2 has been cancelled without prejudice and/or disclaimer.

The claims are amended as follows:

1. (Amended) A tray for storing a semiconductor integrated circuit device having a package and wiring terminals on a lower surface of the package, said tray comprising:

a substantially planar main body; and

a first storage portion provided on a first surface of said main body for storing the semiconductor integrated circuit device, said first storage portion having a first wall surface adapted to be arranged around the semiconductor integrated circuit device when the semiconductor integrated device is stored in said first storage portion,

wherein said first wall surface has a first area and a second area, said first area being [which is] inclined with an angle so as to support an edge of the package of the semiconductor integrated circuit device and to prevent said first wall surface from coming into contact with the wiring terminals of the semiconductor integrated circuit device when the semiconductor integrated circuit device is stored in said first storage portion, and said second area extending

